

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

IN THE CLAIMS

Please amend the claims as follows.

1. (Currently Amended) For use in a data processor, a floating point unit comprising:

a buffer capable of storing operands and comprising a forwarding array of addressable memory locations;

a plurality of floating point processing units capable of executing floating point instructions that write operands to an external memory and capable of executing floating point instructions that read operands from said external memory; and

an operand queue capable of storing a plurality of operands associated with one or more operations being processed in said floating point unit, wherein said operand queue stores a first operand written by a floating point write instruction executed by a first one of said plurality of floating point processing units and wherein said operand queue supplies said first operand to a floating point read instruction executed by a second one of said plurality of floating point processing units when said floating point read instruction requires said first operand; [[.]]

wherein said first operand is virtually committed by writing ~~written~~ the first operand from said operand queue to [[a]] the buffer for storage in an external memory and by writing an operand queue address of the first operand into the memory location in the forwarding array that is associated with the floating point write instruction; ~~and~~

wherein said first operand is supplied to the floating point read instruction by writing the

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

operand queue address of the first operand into the memory location in the forwarding array that is associated with the floating point read instruction, the operand queue address in the memory location associated with the floating point read instruction used to retrieve the first operand from the operand queue; and

wherein a second operand is written directly to the buffer bypassing the operand queue in response to a slot in the operand queue where the second operand was to be stored already being virtually committed.

2. (Previously Presented) The floating point unit as set forth in Claim 1 wherein said floating point unit further comprises a store conversion unit capable of converting operands in said plurality of floating point processing units from an internal format associated with said plurality of floating point processing units to an external format associated with the external memory.

3. (Previously Presented) The floating point unit as set forth in Claim 2 wherein said operand queue receives said first operand from said store conversion unit and transfers said first operand to said buffer for storage in said external memory.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

4. (Previously Presented) The floating point unit as set forth in Claim 1 wherein said floating point unit further comprises a load conversion unit capable of converting incoming operands received from said external memory from an external format associated with an external memory to an internal format associated with said plurality of floating point processing units.

5. (Original) The floating point unit as set forth in Claim 4 wherein said operand queue receives said incoming operands from said external memory and transfers said incoming operands to said load conversion unit.

6. (Original) The floating point unit as set forth in Claim 5 wherein data in said external memory is accessed in groups of N bytes and wherein said floating point unit further comprises at least one aligner capable of receiving a first incoming operand that is misaligned with respect to a boundary between a first N byte group and a second N byte group and aligning said first incoming operand.

7. (Original) The floating point unit as set forth in Claim 6 wherein said operand queue receives said aligned first incoming operand from said at least one aligner.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

8. (Original) The floating point unit as set forth in Claim 7 wherein said at least one aligner sets at least one bit in said operand queue to indicate that said aligned first incoming operand is valid.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

9. (Currently Amended) A data processor comprising:

at least one pipelined integer execution unit;

a data cache;

an instruction cache; and

a floating point unit comprising:

a buffer capable of storing operands and comprising a forwarding array of addressable memory locations;

a plurality of floating point processing units capable of executing floating point instructions that write operands to an external memory and capable of executing floating point instructions that read operands from said external memory; and

an operand queue capable of storing a plurality of operands associated with one or more operations being processed in said floating point unit, wherein said operand queue stores a first operand written by a floating point write instruction executed by a first one of said plurality of floating point processing units and wherein said operand queue supplies said first operand to a floating point read instruction executed by a second one of said plurality of floating point processing units when said floating point read instruction requires said first operand; [[.]]

wherein said first operand is virtually committed by writing ~~written~~ the first operand from said operand queue to [[a]] the buffer for storage in an external memory and by writing an operand queue address of the first operand into the memory location in the forwarding array that is associated with the floating point write instruction; -and

wherein said first operand is supplied to the floating point read instruction by writing the

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

operand queue address of the first operand into the memory location in the forwarding array that is associated with the floating point read instruction, the operand queue address in the memory location associated with the floating point read instruction used to retrieve the first operand from the operand queue; and

wherein a second operand is written directly to the buffer bypassing the operand queue in response to a slot in the operand queue where the second operand was to be stored already being virtually committed.

10. (Previously Presented) The data processor as set forth in Claim 9 wherein said floating point unit further comprises a store conversion unit capable of converting operands in said plurality of floating point processing units from an internal format associated with said plurality of floating point processing units to an external format associated with the external memory.

11. (Previously Presented) The data processor as set forth in Claim 10 wherein said operand queue receives said first operand from said store conversion unit and transfers said first operand to said buffer for storage in said external memory.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

12. (Previously Presented) The data processor as set forth in Claim 9 wherein said floating point unit further comprises a load conversion unit capable of converting incoming operands received from said external memory from an external format associated with an external memory to an internal format associated with said plurality of floating point processing units.

13. (Original) The data processor as set forth in Claim 12 wherein said operand queue receives said incoming operands from said external memory and transfers said incoming operands to said load conversion unit.

14. (Original) The data processor as set forth in Claim 13 wherein data in said external memory is accessed in groups of N bytes and wherein said floating point unit further comprises at least one aligner capable of receiving a first incoming operand that is misaligned with respect to a boundary between a first N byte group and a second N byte group and aligning said first incoming operand.

15. (Original) The data processor as set forth in Claim 14 wherein said operand queue receives said aligned first incoming operand from said at least one aligner.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

16. (Original) The data processor as set forth in Claim 15 wherein said at least one aligner sets at least one bit in said operand queue to indicate that said aligned first incoming operand is valid.

DOCKET NO. P04237
SERIAL NO. 09/877,093
PATENT

17. (Currently Amended) For use in a floating point unit comprising a plurality of floating point processing units capable of executing floating point instructions that write operands to an external memory and capable of executing floating point instructions that read operands from the external memory, a method of accessing the operands comprising:

storing in an operand queue a first operand written by a floating point write instruction executed by a first one of the plurality of floating point processing units;

supplying the first operand from the operand queue to a floating point read instruction executed by a second one of the plurality of floating point processing units when the floating point read instruction requires the first operand, wherein the first operand is supplied to the floating point read instruction by writing an operand queue address of the first operand into a memory location in a forwarding array that is associated with the floating point read instruction, the operand queue address in the memory location associated with the floating point read instruction used to retrieve the first operand from the operand queue;

virtually committing the first operand by writing the first operand from the operand queue to a buffer for storage in the external memory and by writing the operand queue address of the first operand into a memory location in the forwarding array that is associated with the floating point write instruction; and

writing a second operand directly to the buffer bypassing the operand queue in response to a slot in the operand queue where the second operand was to be stored already being virtually committed.

DOCKET NO. P04237
SERIAL NO. 09/477,093
PATENT

18. (Previously Presented) The method as set forth in Claim 17 wherein the floating point unit further comprises a store conversion unit capable of converting operands in the plurality of floating point processing units from an internal format associated with the plurality of floating point processing units to an external format associated with the external memory.

19. (Previously Presented) The method as set forth in Claim 18 further including:

storing the first operand from the store conversion unit into the operand queue.

20. (Previously Presented) The method as set forth in Claim 17 wherein the floating point unit further comprises a load conversion unit capable of converting incoming operands received from an external memory from an external format associated with the external memory to an internal format associated with the plurality of floating point processing units.

21. (Previously Presented) The method as set forth in Claim 20 further including:

storing the incoming operands from the external memory in the operand queue; and
transferring the incoming operands from the operand queue to the load conversion unit.